Appendix B

40-cell Bit Patterns and Timing for SSR(Read/Buck/Boost)

Action	Time	P2 Bit Pattern - Modules 1 & 2																P2 Hex Code	Action	Time
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
Read																				
Zero all outputs		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	00 00		
Settle after turn off	1ms																			
Select cell 1		1	1	0	1	0	0	0	0	1	1	0	1	0	0	0	0	d0d0		
Settle SSR's	5 ms																			
Read cell 1																				
Zero all outputs		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	00 00		
Settle after turn off	1ms																			
Select cell 2		1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	e1e1		
Settle SSR's	5 ms																			
Read cell 2																				
Zero all outputs		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	00 00		
Settle after turn off	1ms																			
Select cell 3		1	1	0	1	0	0	1	0	1	1	0	1	0	0	1	0	d2d2		
Settle SSR's	5 ms																			
Read cell 3																				
Zero all outputs		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	00 00		
Settle after turn off	1ms																			
Select cell 4		1	1	1	0	0	0	1	1	1	1	1	0	0	0	1	1	e3e3		
Settle SSR's	5 ms																			
Read cell 4																				
Zero all outputs		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	00 00		
Settle after turn off	1ms																			
Select cell 5		1	1	0	1	0	1	0	0	1	1	0	1	0	1	0	0	d4d4		
Settle SSR's	5 ms																			

40-cell Bit Patterns and Timing for SSR(Read/Buck/Boost)

Action	Time	P2 Bit Pattern - Modules 1 & 2																P2 Hex Code	Action	Time
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
Read cell 5																				
Zero all outputs		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	00 00		
Settle after turn off	1ms																			
Select cell 6		1	1	1	0	0	1	0	1	1	1	1	0	0	1	0	1	e5e5		
Settle SSR's	5 ms																			
Read cell 6																				
Zero all outputs		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	00 00		
Settle after turn off	1ms																			
Select cell 7		1	1	0	1	0	1	1	0	1	1	0	1	0	1	1	0	d6d6		
Settle SSR's	5ms																			
Read cell 7																				
Zero all outputs		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	00 00		
Settle after turn off	1ms																			
Select cell 8		1	1	1	0	0	1	1	1	1	1	1	0	0	1	1	1	e7e7		
Settle SSR's	5ms																			
Read cell 8																				
Zero all outputs		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	00 00		
Settle after turn off	1ms																			
Select cell 9		1	1	0	1	1	0	0	0	1	1	0	1	1	0	0	0	d8d8		
Settle SSR's	5ms																			
Read cell 9																				
Zero all outputs		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	00 00		
Settle after turn off	1ms																			
Select cell 10		1	1	1	0	1	0	0	1	1	1	1	0	1	0	0	1	e9e9		
Settle SSR's	5 ms																			
Read cell 10																				
Bucking																				
Zero all outputs		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	00 00		
Settle after turn off	1ms																			
Select cell 1		1	0	0	1	0	0	0	0	1	0	0	1	0	0	0	0	9090		
Settle SSR's	5 ms																			
Read cell 1																				

40-cell Bit Patterns and Timing for SSR(Read/Buck/Boost)

Action	Time	P2 Bit Pattern - Modules 1 & 2																P2 Hex Code	Action	Time
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
Zero all outputs		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	00 00		
Settle after turn off	1ms																			
Select cell 2		1	0	1	0	0	0	0	1	1	0	1	0	0	0	0	1	a1a1		
Settle SSR's	5 ms																			
Read cell 2																				
Zero all outputs		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	00 00		
Settle after turn off	1ms																			
Select cell 3		1	0	0	1	0	0	1	0	1	0	0	1	0	0	1	0	9292		
Settle SSR's	5 ms																			
Read cell 3																				
Zero all outputs		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	00 00		
Settle after turn off	1ms																			
Select cell 4		1	0	1	0	0	0	1	1	1	0	1	0	0	0	1	1	a3a3		
Settle SSR's	5 ms																			
Read cell 4																				
Zero all outputs		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	00 00		
Settle after turn off	1ms																			
Select cell 5		1	0	0	1	0	1	0	0	1	0	0	1	0	1	0	0	9494		
Settle SSR's	5 ms																			
Read cell 5																				
Zero all outputs		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	00 00		
Settle after turn off	1ms																			
Select cell 6		1	0	1	0	0	1	0	1	1	0	1	0	0	1	0	1	a5a5		
Settle SSR's	5 ms																			
Read cell 6																				
Zero all outputs		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	00 00		
Settle after turn off	1ms																			
Select cell 7		1	0	0	1	0	1	1	0	1	0	0	1	0	1	1	0	9696		
Settle SSR's	5ms																			
Read cell 7																				
Zero all outputs		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	00 00		
Settle after turn off	1ms																			

40-cell Bit Patterns and Timing for SSR(Read/Buck/Boost)

Action	Time	P2 Bit Pattern - Modules 1 & 2																P2 Hex Code	Action	Time
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
Select cell 8		1	0	1	0	0	1	1	1	1	0	1	0	0	1	1	1	a7a7		
Settle SSR's	5ms																			
Read cell 8																				
Zero all outputs		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	00 00		
Settle after turn off	1ms																			
Select cell 9		1	0	0	1	1	0	0	0	1	0	0	1	1	0	0	0	9898		
Settle SSR's	5ms																			
Read cell 9																				
Zero all outputs		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	00 00		
Settle after turn off	1ms																			
Select cell 10		1	0	1	0	1	0	0	1	1	0	1	0	1	0	0	1	a9a9		
Settle SSR's	5 ms																			
Read cell 10																				
Boosting																				
Zero all outputs		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	00 00		
Settle after turn off	1ms																			
Select cell 1		0	1	0	1	0	0	0	0	0	1	0	1	0	0	0	0	5050		
Settle SSR's	5 ms																			
Read cell 1																				
Zero all outputs		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	00 00		
Settle after turn off	1ms																			
Select cell 2		0	1	1	0	0	0	0	1	0	1	1	0	0	0	0	1	6161		
Settle SSR's	5 ms																			
Read cell 2																				
Zero all outputs		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	00 00		
Settle after turn off	1ms																			
Select cell 3		0	1	0	1	0	0	1	0	0	1	0	1	0	0	1	0	5252		
Settle SSR's	5 ms																			
Read cell 3																				
Zero all outputs		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	00 00		
Settle after turn off	1ms																			
Select cell 4		0	1	1	0	0	0	1	1	0	1	1	0	0	0	1	1	6363		

40-cell Bit Patterns and Timing for SSR(Read/Buck/Boost)

Action	Time	P2 Bit Pattern - Modules 1 & 2																P2 Hex Code	Action	Time
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
Settle SSR's	5 ms																			
Read cell 4																				
Zero all outputs		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	00 00		
Settle after turn off	1ms																			
Select cell 5		0	1	0	1	0	1	0	0	0	1	0	1	0	1	0	0	5454		
Settle SSR's	5 ms																			
Read cell 5																				
Zero all outputs		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	00 00		
Settle after turn off	1ms																			
Select cell 6		0	1	1	0	0	1	0	1	0	1	1	0	0	1	0	1	6565		
Settle SSR's	5 ms																			
Read cell 6																				
Zero all outputs		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	00 00		
Settle after turn off	1ms																			
Select cell 7		0	1	0	1	0	1	1	0	0	1	0	1	0	1	1	0	5656		
Settle SSR's	5ms																			
Read cell 7																				
Zero all outputs		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	00 00		
Settle after turn off	1ms																			
Select cell 8		0	1	1	0	0	1	1	1	0	1	1	0	0	1	1	1	6767		
Settle SSR's	5ms																			
Read cell 8																				
Zero all outputs		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	00 00		
Settle after turn off	1ms																			
Select cell 9		0	1	0	1	1	0	0	0	0	1	0	1	1	0	0	0	5858		
Settle SSR's	5ms																			
Read cell 9																				
Zero all outputs		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	00 00		
Settle after turn off	1ms																			
Select cell 10		0	1	1	0	1	0	0	1	0	1	1	0	1	0	0	1	6969		
Settle SSR's	5 ms																			
Read cell 10																				

Additional Bit Patterns for Ports 7 & 8

P7 Bit Pattern - Module 3								P7 Hex Code	Action	Time	P8 Bit Pattern - Module 4								P8 Hex Code
7	6	5	4	3	2	1	0				7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	00			0	0	0	0	0	0	0	0	00
1	1	0	1	0	0	0	0	d0			1	1	0	1	0	0	0	0	d0
0	0	0	0	0	0	0	0	00			0	0	0	0	0	0	0	0	00
1	1	1	0	0	0	0	1	e1			1	1	1	0	0	0	0	1	e1
0	0	0	0	0	0	0	0	00			0	0	0	0	0	0	0	0	00
1	1	0	1	0	0	1	0	d2			1	1	0	1	0	0	1	0	d2
0	0	0	0	0	0	0	0	00			0	0	0	0	0	0	0	0	00
1	1	1	0	0	0	1	1	e3			1	1	1	0	0	0	1	1	e3
0	0	0	0	0	0	0	0	00			0	0	0	0	0	0	0	0	00
1	1	0	1	0	1	0	0	d4			1	1	0	1	0	1	0	0	d4

Additional Bit Patterns for Ports 7 & 8

P7 Bit Pattern - Module 3								P7 Hex Code	Action	Time	P8 Bit Pattern - Module 4								P8 Hex Code
7	6	5	4	3	2	1	0				7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	00			0	0	0	0	0	0	0	0	00
1	1	1	0	0	1	0	1	e5			1	1	1	0	0	1	0	1	e5
0	0	0	0	0	0	0	0	00			0	0	0	0	0	0	0	0	00
1	1	0	1	0	1	1	0	d6			1	1	0	1	0	1	1	0	d6
0	0	0	0	0	0	0	0	00			0	0	0	0	0	0	0	0	00
1	1	1	0	0	1	1	1	e7			1	1	1	0	0	1	1	1	e7
0	0	0	0	0	0	0	0	00			0	0	0	0	0	0	0	0	00
1	1	0	1	1	0	0	0	d8			1	1	0	1	1	0	0	0	d8
0	0	0	0	0	0	0	0	00			0	0	0	0	0	0	0	0	00
1	1	1	0	1	0	0	1	e9			1	1	1	0	1	0	0	1	e9
0	0	0	0	0	0	0	0	00			0	0	0	0	0	0	0	0	00
1	0	0	1	0	0	0	0	90			1	0	0	1	0	0	0	0	90

Additional Bit Patterns for Ports 7 & 8

P7 Bit Pattern - Module 3								P7 Hex Code	Action	Time	P8 Bit Pattern - Module 4								P8 Hex Code
7	6	5	4	3	2	1	0				7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	00			0	0	0	0	0	0	0	0	00
1	0	1	0	0	0	0	1	a1			1	0	1	0	0	0	0	1	a1
0	0	0	0	0	0	0	0	00			0	0	0	0	0	0	0	0	00
1	0	0	1	0	0	1	0	92			1	0	0	1	0	0	1	0	92
0	0	0	0	0	0	0	0	00			0	0	0	0	0	0	0	0	00
1	0	1	0	0	0	1	1	a3			1	0	1	0	0	0	1	1	a3
0	0	0	0	0	0	0	0	00			0	0	0	0	0	0	0	0	00
1	0	0	1	0	1	0	0	94			1	0	0	1	0	1	0	0	94
0	0	0	0	0	0	0	0	00			0	0	0	0	0	0	0	0	00
1	0	1	0	0	1	0	1	a5			1	0	1	0	0	1	0	1	a5
0	0	0	0	0	0	0	0	00			0	0	0	0	0	0	0	0	00
1	0	0	1	0	1	1	0	96			1	0	0	1	0	1	1	0	96
0	0	0	0	0	0	0	0	00			0	0	0	0	0	0	0	0	00

Additional Bit Patterns for Ports 7 & 8

P7 Bit Pattern - Module 3								P7 Hex Code	Action	Time	P8 Bit Pattern - Module 4								P8 Hex Code
7	6	5	4	3	2	1	0				7	6	5	4	3	2	1	0	
1	0	1	0	0	1	1	1	a7			1	0	1	0	0	1	1	1	a7
0	0	0	0	0	0	0	0	00			0	0	0	0	0	0	0	0	00
1	0	0	1	1	0	0	0	98			1	0	0	1	1	0	0	0	98
0	0	0	0	0	0	0	0	00			0	0	0	0	0	0	0	0	00
1	0	1	0	1	0	0	1	a9			1	0	1	0	1	0	0	1	a9
0	0	0	0	0	0	0	0	00			0	0	0	0	0	0	0	0	00
0	1	0	1	0	0	0	0	50			0	1	0	1	0	0	0	0	50
0	0	0	0	0	0	0	0	00			0	0	0	0	0	0	0	0	00
0	1	1	0	0	0	0	1	61			0	1	1	0	0	0	0	1	61
0	0	0	0	0	0	0	0	00			0	0	0	0	0	0	0	0	00
0	1	0	1	0	0	1	0	52			0	1	0	1	0	0	1	0	52
0	0	0	0	0	0	0	0	00			0	0	0	0	0	0	0	0	00
0	1	1	0	0	0	1	1	63			0	1	1	0	0	0	1	1	63

Additional Bit Patterns for Ports 7 & 8

P7 Bit Pattern - Module 3								P7 Hex Code	Action	Time	P8 Bit Pattern - Module 4								P8 Hex Code
7	6	5	4	3	2	1	0				7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	00			0	0	0	0	0	0	0	0	00
0	1	0	1	0	1	0	0	54			0	1	0	1	0	1	0	0	54
0	0	0	0	0	0	0	0	00			0	0	0	0	0	0	0	0	00
0	1	1	0	0	1	0	1	65			0	1	1	0	0	1	0	1	65
0	0	0	0	0	0	0	0	00			0	0	0	0	0	0	0	0	00
0	1	0	1	0	1	1	0	56			0	1	0	1	0	1	1	0	56
0	0	0	0	0	0	0	0	00			0	0	0	0	0	0	0	0	00
0	1	1	0	0	1	1	1	67			0	1	1	0	0	1	1	1	67
0	0	0	0	0	0	0	0	00			0	0	0	0	0	0	0	0	00
0	1	0	1	1	0	0	0	58			0	1	0	1	1	0	0	0	58
0	0	0	0	0	0	0	0	00			0	0	0	0	0	0	0	0	00
0	1	1	0	1	0	0	1	69			0	1	1	0	1	0	0	1	69